LOW POWER DIGITAL PULSE CONTROLLER BY PULSE WIDTH MODULATOR

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ABSTRACT
A digitally controlled current starved pulse width modulator (PWM) is described in this paper. The current from the power grid to the ring oscillator is controlled by a header circuit. By changing the header current, the pulse width of the switching signal generated at the output of the ring oscillator is dynamically controlled, permitting the duty cycle to vary between 25% and 90%. This low-power embedded microprocessor, fabricated with 0.18-μm CMOS embedded DRAM technology, enables high-performance operations such as audio and video application.

Keywords—Current starvation, digital-controlled oscillators, pulse width modulation, ring oscillators.

I. INTRODUCTION
Voltage Controlled Oscillators (VCOs) are widely used to generate a switching signal where certain characteristics of this signal can be controlled. Two types of VCOs are primarily used in high-performance integrated circuits (ICs), inductor-capacitor (LC) oscillators, and ring oscillators. LC oscillators can operate at high frequencies and exhibit superior noise performance. Alternatively, ring oscillator occupy smaller on-chip area with a wider tuning range.

Fig1- Ring oscillator with current controlled Podd and Peven transistors.

This type of application must achieve long system lifetimes from a limited energy source, so the need to reduce energy consumption whenever possible is paramount. Dynamic voltage scaling (DVS) has become a standard approach for reducing power when performance requirements vary. Our approach offers both dynamic frequency control (DFC) and dynamic voltage control (DVC). Clock frequency is autonomously and dynamically controlled while supply voltage is adaptively controlled resulting in the leakage power compensation effect.

This dynamic voltage and frequency management (DVFM) approach achieved 82% power reduction in a Personal Information Management (PIM) application. Handheld audio and video applications require high-performance and low-power processor hardware. In the case of a multi-application product such as a PDA, performance and power requirements vary widely, depending on the application being run. For example, the targeted power consumption for a move application is typically 250 mW, 75 mW for an audio application, 50 mW for a schedule application, and 3 mW for standby mode.

A conventional ring oscillator consists of an odd number of inverters where the output of the last inverter is fed back to the input of the first inverter, as shown in Fig. 1. The delay provided by each inverter in this chain produces a phase shift in the switching signal. The sum of these individual delays (i.e., phase shifts) and the feedback from the last to the first inverter produces a total phase shift of 2π that causes the circuit to oscillate.

The frequency of this oscillation depends upon the sum of the inverter delays within the chain. The duty cycle of the generated switching signal is typically 50% for conventional ring oscillators where the pMOS and nMOS transistors within the inverters provide the same rise and fall transition times. The duty cycle of a ring oscillator can be tuned by controlling the transition time of the inverters within the ring oscillator. Header and footer circuits are widely used to control the current
supplied to the pMOS and nMOS transistors within the ring oscillator inverter chain. Although the header and footer circuits are typically used to control the frequency, these circuits can also control the duty cycle of a ring oscillator.

The fluctuations in operation speed and power consumption also become serious. Also, the increase of power consumption by the sub threshold leakage is a critical problem for battery-driven devices.

General methods of power reduction are voltage scaling and lowering the operating clock frequency. In our DVFM approach, clock frequency is autonomously and dynamically controlled while voltage is adaptively controlled at the same time. A delay synthesizer in the DVC circuit emulates and provides the circuit delay information while the DFC circuit determines optimum operating frequency for the microprocessor to perform desired functions efficiently.

To lower the operating frequency, this microprocessor incorporates a 2D graphics engine, a DSP core, and a 128-bit wideband bus architecture with 64-Mb of embedded DRAM.

Section II explains the design concepts used to simultaneously achieve high-performance and low-power consumption. Section III describes in detail the techniques used in our DVFM scheme to achieve low power consumption and leakage-compensation effect. Section IV reports the magnitude of power reduction achieved through use of the DVFM. Additionally, a DC2V converter, based on the frequency to voltage converter proposed in [9] is used as a DC2V converter. The DFC block controls the clock frequency at the required minimum value autonomously in hardware without special power-management software.

II. DESCRIPTION OF THE PROPOSED PWM ARCHITECTURE

2.1. Header Circuitry.

This circuit is used, as a header in to compensate for temperature and process variations by maintaining a constant current to the ring oscillator. Gates $M_1$ and $M_2$ are controlled by the analog signal $C_a$. As opposed to a single transistor $M_3$ whose gate is connected to a resistor, as shown in Fig. 3,
There are primarily three different phases of this circuit. During the first phase, capacitor C1 is charged through transistor P1. In the second phase, transistors (i.e., switches) N2 and N3 are turned on to allow charge sharing between C1 and C2. During the last phase, C1 is discharged through N1.

Many signal processing systems process blocks of data that arrive at some regular rate, and sometimes the amount of data to process is less than the maximum amount. shows four approaches to power supply management for reducing energy consumption when the workload varies [1]. It plots the required rate of the system versus the normalized Energy required to process one generic block of data.

The charge time of C1 depends upon the duty cycle of the input switching signal. A signal with a greater duty cycle causes more charge to accumulate on C1, increasing the output voltage of the DC2V converter. The proposed DC2V converter controls the bias current from the header circuitry through negative feedback, mitigating PVT variations. Intuitively, when the header current is reduced, the duty cycle of the ring oscillator is greater, increasing the output voltage of the DC2V converter.

The most straightforward method for saving energy when the workload decreases is to operate at the maximum rate until all of the required processing is complete and then to shutdown. This approach only requires a single power supply voltage (corresponding to full rate operation), and it results in linear energy savings.

2.3. Ring Oscillator Topology for Pulse Width Modulation.

To create a single low-to-high oscillation at the output of the ring oscillator, the signal propagates twice through the entire ring oscillator stages.

\[ P = T_{\text{high}} + T_{\text{low}} \]

Ring oscillator is cascaded combination of delay stages, connected in a close loop chain.

The ring oscillators designed with a chain of delay stages have created great interest because of their numerous useful features. These attractive features are:

(i) It can be easily designed with the state-of-art integrated circuit technology (CMOS, BiCMOS), (ii) It can achieve its oscillations at low voltage, (iii) It can provide high frequency oscillations with dissipating low power, (iv) It can be electrically tuned, (v) It can provide wide tuning range and (vi) It can provide multiphase outputs because of their basic structure.

To achieve self-sustained oscillation, the ring must provide a phase shift of 2π and have unity voltage gain at the frequency of oscillation. All of the MOSFET transistors are designed with similar rise and fall transition times, contributing equally to the high and low portions of the output signal. The half period of a conventional 50% duty cycle \((T_0, \text{high} = T_0, \text{low})\) ring oscillator with \(2m + 1\) stages The NMOS transistor changes from the saturation to linear mode of operation during the high to low transition at \(v_{\text{out}}=VDD-v_{TN}\) while \(v_{\text{in}}=VDD\) during this entire transition.

High Speed Ring Topology.

The increase of oscillation frequency can be achieved in two ways: by reducing the propagation time delay of inverter stages or by decreasing the number of stages used in the ring structure. Three popular high speed ring structures are: (i) negative skewed delay ring oscillator, (ii) multi-feedback ring oscillator and (iii) coupled ring oscillator.

2.4. Ring Oscillator Topology for Pulse Width Modulation with Constant Frequency.

The duty cycle of a switching signal can be controlled by changing the current to the odd (or even) stages of a conventional ring oscillator, as demonstrated in Section II-C. Consider a ring oscillator with \(2m + 1\) stages and two headers \(HA\) and \(HB\) that supply, respectively, the current \(I_{\text{bias}}, A = I_{\text{ave}}\) to the \(m + 1\) low \(P_{\text{odd}}\) transistors and \(I_{\text{bias}}, B = \beta I_{\text{ave}}\) to the \(m\) even transistors,

![Fig.4-Parallel pMOS transistors replace M3 to improve the granularity of the current control as well as behave as switch transistors to turn on different sections of the header circuitry.](image-url)

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III. SIMULATION RESULTS

The proposed circuit is designed in a 22-nm CMOS predictive technology model (PTM).
3.1. Monte Carlo method

Monte Carlo methods (or Monte Carlo experiments) are a broad class of computational algorithms that rely on repeated random sampling to obtain numerical results; Monte Carlo methods are mainly used in three distinct problem classes: optimization, numerical integration and generation of draws from a probability distribution.

3.2. Proposed PWM under PVT Variations

Monte Carlo simulation’ is more specifically used to describe a method for propagating (translating) uncertainties in model inputs into uncertainties in model outputs. It is a type of simulation that explicitly and quantitatively represents uncertainties. Monte Carlo simulation relies on the process of explicitly representing uncertainties by specifying inputs as probability distributions.

3.3. Duty Cycle Controlled PWM

The accuracy of the analytic expressions of the duty cycle presented in Section II-C is evaluated in this section for a wide 25% to 90% range of duty cycle.

3.4 Duty Cycle and Frequency Controlled PWM

The current supply to the ring oscillator is controlled with two headers, exhibiting a frequency of 8.33 MHz 1.25% for all the values of duty cycle. In the conventional design technique that does not use wideband bus architecture; the power consumption is 741 mW.

IV. CONCLUSIONS

A digitally controlled PWM with a wide pulse width range of 25% to 90% is proposed in this paper. Local voltage dithering provides a flexible approach for saving energy in fixed throughput systems. Here using both analog and digital techniques so using analog filter to reduce noise. Delay 10% to 20% will be reduced and using Monte Carlo simulation method will be used in this paper.

REFERENCES


Fig. 5 Header current I_{bias,A} changes from 40 to 11 μA. (a) Duty cycle varies between 25% and 90% (error < 3.1%). (b) Period remains approximately constant (error < 1.25%).

The power was reduced by 53%. Moreover, the DVFM optimizes the operating frequency and the supply voltage, resulting in the final power consumption of 210 mW, enabling long movie playback on a portable device.

<table>
<thead>
<tr>
<th>COMPUTATION OF PARAMETER</th>
<th>PWM</th>
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<tbody>
<tr>
<td>AVERAGE POWER</td>
<td>3.54 mW</td>
</tr>
<tr>
<td>STATIC POWER</td>
<td>3.96 MW</td>
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<tr>
<td>STATIC CURRENT</td>
<td>2.20 MA</td>
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<tr>
<td>PDP</td>
<td>158.52 NWS</td>
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<tr>
<td>EDP</td>
<td>6.34 PWS</td>
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<tr>
<td>AREA OF TRANSISTOR</td>
<td>381.25 mm^2</td>
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