DESIGN AND IMPLEMENTATION OF AN IMPROVED CHARGE PUMP USING VOLTAGE DOUBLER AS CLOCK SCHEME

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Abstract

Charge pumps are circuits that can pump charge upwards to produce voltages higher than the regular supply voltage. Novel MOS charges pump utilizing Voltage Doubler for producing clock which is double the magnitude that of input voltage supply. In this proposed paper by using Voltage Doubler as clock scheme the clocks produced in voltage form are amplified increasing the potential at every node of the circuit. By using this structure fewer charge pump stages are required to obtain the required output voltage. This Present charge pump circuit is implemented as a combination of charge pump using dynamic charge transfer switches and Voltage Doubler in this work using 0.25µm technology in Mentor Graphics DA-IC Station 2008.2o. A four stage enhanced charge pump is designed to produce 7-8V output from a 1V supply using non-overlapping clock signal generated by Voltage Doubler that drive the charge pump circuit.

Key Words: Dual watermarking, spatial domain, frequency domain.

I. INTRODUCTION

Charge pumps are DC to DC converters designed to improve the overall voltage gain. It uses capacitors for storing the energy. Charge pump circuits are capable of providing high efficiencies[1]. They can generate output voltage of several times higher than voltage supply VDD. Several devices (such as LCD displays, non volatile memories and many small power devices). These devices required integrated DC-DC voltage converters also referred as voltage elevators. Charge pumps are widely used in non volatile memories such as EEPROM and flash memories. In the recent years attempts have been made towards small, inexpensive efficient mobile computing [4]. In this paper, a new charge pump is proposed to meet the need of higher voltage in the smart power devices. This paper is organized in following sections as follows: introduction in the I, Dickson charge pump – II, charge pump using static charge transfer switches in III, charge pump using dynamic charge transfer switches- IV, charge pump using PGI-V, Voltage Doubler circuit - VI, proposed circuit - VII, simulation results – VIII, conclusion and future scope – IX.

II. DICKSON CHARGE PUMP

Dickson charge pump is the basic kind of charge pump upon which other modification follows. Dickson charge pump earlier was implemented using diodes as switches and capacitor in parallel. The basic configuration of the Dickson circuit is shown in figure 1. All the diodes and capacitor chosen are identical i.e. they are of same geometrical dimension. The principle behind the charge pumping in this architecture is boosting of charge across capacitor alternatively with the help of non-overlapping clock[3]. The top plate of each capacitor is connected to the output node of every nMOS transistor whereas the bottom plate is driven by the complementary clock as shown in the figure below.

![Figure 1 Dickson Charge Pump using Diodes](image-url)
The charge pump is implemented using diode-connected nMOS transistors. Here the diode voltage is replaced by the MOS threshold voltage, $V_{thn}$.

The voltage pumping gain, $G_V$, of the charge pump is delineated as:

$$ G_V = V_{N+1} - V_N = \Delta V - V_{thn} $$  (4)

### III. CHARGE PUMP USING CTS (NCP-1)

Jieh-Tsorng Wu gives design for charge pump using static charge transfer switches also named as New Charge Pump-1 (NCP-1) uses static switches to enhance the voltage gain of each stage. The basic idea behind this approach is to use MOS switches with proper ON/OFF characteristics to direct charge pump flow during pumping operation. MOS switches perform better than diodes or diode connected nMOS transistors which unnecessarily introduces a forward voltage drop at each node[3]. One of the first low voltage CTS based charge pump with static backward control. In this circuit design high voltage established at the next voltage is used back to the gate of first stages’ CTS. This will work if the switches can be switched ON and switched OFF at correct timings so as to transfer the charge properly in only one direction.

If compared with Dickson Charge pump gain of each stage, gain of NCP-1 is found to be better and it also eliminates the problem of threshold voltage drop. We can see that the NCP – 1 charge pump presented by Wu is much more suitable for low voltage than the Dickson charge pump[4].

The voltage pumping gain of the static charge pump now becomes

$$ G_V = V_2 - V_1 = \Delta V $$  (5)

If compared with Dickson Charge pump gain of each stage, gain of NCP-1 is found to be better and it also eliminates the problem of threshold voltage drop. We can see that the NCP – 1 charge pump presented by Wu is much more suitable for low voltage than the Dickson charge pump. However, the inclusion of auxiliary switching devices creates a path to leak the charges stored in the high voltage nodes. This fact may cause some loss of charges during pumping and extend the time for each node to achieve their ideal voltage level [9].
IV. CHARGE PUMP USING DYNAMIC CTS (NCP-2)

Charge pump using Dynamic charge transfer switches (NCP-2) is the improved version of charge pump static CTS. NCP-1 suffers from the problem of reverse charge leakage because of the CTS which remain in ON state for the entire operation giving path for the charges to leak out. Thus a new charge pump circuit has been developed by adding pMOS and nMOS. Each CTS is combined with an auxiliary pass transistors so as to turn the CTS ON and OFF at designated time[4].

![Figure 6 A four stage charge pump using dynamic CTS (NCP-2)](image)

V. CHARGE PUMPS WITH PUMPING GAIN INCREASE CIRCUITS (PGI)

If the problem of limitation of the diode configured output stage can be eliminated better pumping performance can be achieved. So, a novel MOS charge pump using pumping gain increase (PGI) circuits with high voltage transfer efficiency to generate boosted output voltages [5]. This structure of charge pump is shown in Figure 14. In PGI circuit the output circuit is replaced with an pMOS switch named as MSO. The control circuit is omitted by connecting the gate of MSO to the gate of previous stage CTS. This structure of charge pump is shown in Figure 7. By using the PGI circuits, the threshold voltage problem of the MOSFET is solved, and also, the limitation of the diode-configured output stage is removed. Thus, the boosted output voltage increases.

![Figure 7 One-stage charge pump circuit using PGI](image)

VI. VOLTAGE DOUBLER

In this circuit, the amplitude of the clock and the power supply is made to oscillate between 0 ~ VDD. The transistor M1 on receiving high state remains off showing low output on VOUT2 but when the clock is transited from VDD to 0V the capacitor C2 changes its state from 0V to VDD. Owing to the charging of the previous clock state on the capacitor C2, the voltage if the anode plate if the capacitor C2 would become 2VDD. So the output voltage of Vout2 would be switched between VDD to 2VDD during the clock was activated. The pMOS of the inverter is connected to the source node of M2 and the CMOS inverter is controlled by the clock itself. As the clock was at VDD, M8 would be turn on discharging the output of the inverter to 0V [7]. Now when the clock is low this would make the pMOS operative giving on 2VDD and its source voltage is 2VDD. The source voltage (2VDD) of the transistor M7 would charge the output capacitor of the inverter. This doubled potential of the will double the output node of the inverter i.e. 2VDD. So, the value of Vout4 oscillated between 0V to 2VDD during the action of clock. The left hand of the circuit showed similar operation principle with opposite polarity.

![Figure 8 Voltage Doubler](image)
VII. PROPOSED CIRCUIT

In the proposed circuit, one stage of Voltage Doubler discussed above is connected to each stage of the charge pump via bottom plate of the capacitor. The output clock voltage of each stage was applied to two places. First, it was to be the pumping clock of the nMOS diode in the charge pump using dynamic CTS structure. Second, it provided clock scheme to the following stage of the clock Voltage Doubler to produce higher amplitude of clock voltage. In the clock scheme, Voltage Doubler was connected stage by stage. The high output voltage of first stage was 2VDD as discussed in previous. The high output voltage of the second stage was increased to 3VDD and the high output voltage of the third stage was increased to 4VDD. So, the output voltage of each stage was increased as stage of the clock Voltage Doubler was increased.

VIII. SIMULATION RESULTS

Present charge pump circuit is implemented using the multi stage voltage Doubler scheme. Here is shown multi-staged Voltage Doubler charge pump circuit with its simulation result.

Charge pump circuit is implemented on the Mentor Graphics DA-IC station with specification as follows:
- Pumping capacitor = 50 pF
- Load capacitor = 0.5 pF
- Supply voltage = 1V
- Output voltage = 7.22 V
- Total Power dissipation = 158.7504pWatts

This is the final circuit developed with its clocking scheme replaced from conventional clock to the multi-staged Voltage Doubler circuit. Multi-staged Voltage Doubler circuit produces doubled out as the clock which further alternatively drives the charge pump giving out double the output voltage. The output voltage has been increased from 4.26 V to 7.22 V and the total power dissipation 158.7504pWatts with the same parameters of capacitance, input voltage, geometrical dimensions.
IX. CONCLUSION AND FUTURE SCOPE

CONCLUSION
This paper presented technique to improve the performance and conversion efficiency of charge pump. Multistage voltage doubler circuit increases the input clock to the charge pump circuit thereby increasing the output voltage. The Present technique uses conventional charge pump with Pumping Gain Increase (PGI) Circuit driven by Voltage Doubler and is suitable for building high-efficiency circuit. This work is a combination of two basic charge pumps to develop a new and better performing charge pump to meet new age applications requirement. Changing the regular clocking circuit with enhanced clock circuit which uses Voltage Doubler to produce doubles the voltages than input supply in the Pumping Gain Increase (PGI) Circuit gives 69% improved response. The present architecture is designed in Mentor Graphics DA-IC 2008.2o station on 0.25µm technology.

FUTURE SCOPE
The future work includes verifying the simulation results of charge pump using Voltage Doubler as clock generator and verifying the simulation results, improving the output voltage of the Present design. A charge recycling principle may be implemented to improve the power dissipation of the charge pump circuit. Charge reuse can be applied to the base circuit of charge pump with Pumping Gain Increase (PGI) Circuit or to the Present design of the charge pump and to any properly driven charge pumps. A significant portion of the charges normally wasted through parasitic capacitances can be reused by means of small additional switch and control signals easily generated from non overlapping phases.

REFERENCES