Investigation of THD in Seven-Level Single-Phase Diode Clamped Multi-Level Inverter at Varying Modulation Index Using Different SPWM Control Strategies

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ABSTRACT
This work proposes the optimization of the single phase seven level diode clamp multi-level inverter using Phase opposition disposition (POD), Alternate phase opposition disposition (APOD) and Phase disposition (PD) at varying modulation index (m_i) of 0.6 to 1.0.The result obtained for THD of the DCMLI using PD SPWM for modulation index of 0.6, 0.7, 0.8, 0.9, and 1 are 32.88 %, 24.86 %, 23.97 %, 22.11 % and 17.93 %. For POD SPWM, the THD result for the same range of modulation index are 32.86 %, 24.84 %, 23.96 %, 22.09 %, and 17.91 % respectively. For APOD SPWM, the THD result for the same range of modulation index are 32.82 %, 24.85 %, 23.97 %, 22.12 %, and 17.89 % respectively. From the results obtained, the APOD SPWM has the lowest THD of 17.89 % at a modulation index of 1.0. in the MATLAB/SIMULINK environment.

Keywords–*Alternate phase opposition disposition (APOD), Phase disposition (PD), Phase opposition disposition (POD), Pulse width modulation (PWM),Total harmonic distortion (THD)*

1.0 INTRODUCTION
The input voltage, output voltage and frequency of an inverter depend on the design of the circuit. A power inverter can be entirely electronic or may be a combination of mechanical effects and electronic circuit [1].
There are different types of power converters which include: DC-DC converters, DC-AC converters (inverters), AC-DC converters (rectifiers) and AC-AC converters [2]. Converters have become more and more common over the past several years as support for self-sufficient power has increased.

1.1 Multi-Level Inverters
Multilevel Inverter (MLI) topologies have been widely used in the motor drive industry to run induction machines for high power and high voltage configurations [3].
MLIs divide the main DC supply voltage into several DC sources which are used to synthesize an AC voltage into a stepped approximation of the desired sinusoidal waveform. The stepped approximation is also popularly known as the staircase model [4]. The number of stages helps decide the power capacity of the Inverter as a whole. Suitable connections either in series or shunt mode or both are done to achieve higher voltage and/or current ratings. MLCs offer several advantages in terms of high power capability, transformer less operation, short-circuit protection, and excellent quality of output current waveform [5] and [6].

2.0 DESIGN AND ANALYSIS
2.1 System Block Diagram
Fig. 1 shows the block diagram of a single phase seven level Diode Clamp multi-level inverter. The battery array generates the required DC voltage of $220V_{dc}$ that the boost converter steps up to $630V_{dc}$ which is controlled by PI controller. The step up voltage is fed into a single phase seven level Diode Clamp MLI using optimized APOD SPWM to generate switching pulses for the inverter switches which produce a seven level output voltage of $220V_{ac}$ for household load.

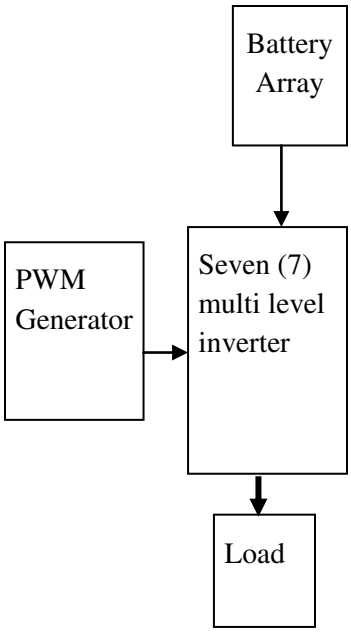

Figure 1: The block diagram of the single phase seven level Diode Clamp inverter.

2.2 Circuit Configuration and Operational Principle

The circuit in Fig. 2 shows a single phase seven level DCMLI which uses twelve (12) power semiconductor switches, six (6) DC link capacitors and ten (10) clamping diodes. This DCMLI consists of four switching pairs (S_1, S_7), (S_2, S_8), (S_3, S_9), (S_4, S_{10}), (S_5, S_{11}) and (S_6, S_{12}). If one switch of the pair is switched on, the other complementary switch of same pair must be off. The DC-link capacitors together with the diodes clamp the switching voltage to half level of the DC bus voltage while the neutral (N) is the reference point of the circuit. Typical switch combinations to obtain the required output voltage levels for seven-level DCMLI are as shown in Table 1.

In the circuit configuration of the single phase seven level DCMLI, each inverter phase is powered by a single DC source. With the appropriate switching of the semi-conductor switches in the modules, each of the phases produces seven output voltage levels. The switching patterns for the different voltage levels are as presented in Table 1.

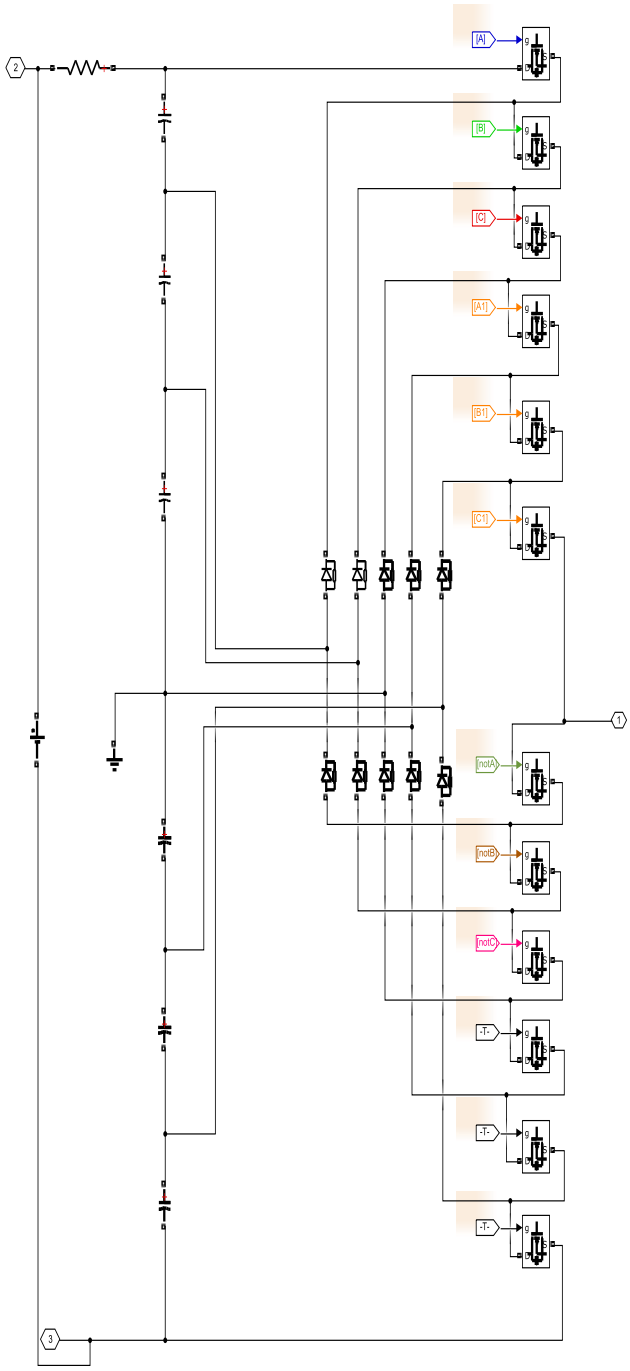

Figure 2: Single-phase Seven-Level Diode Clamped MLI

Table 1: Switching states of a Seven-level DC MLI

Output Voltage Level	Switching States											
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
Vdc/2	1	1	1	1	1	1	0	0	0	0	0	0
Vdc/3	0	1	1	1	1	1	1	0	0	0	0	0
Vdc/6	0	0	1	1	1	1	1	1	0	0	0	0
0	0	0	0	1	1	1	1	1	1	0	0	0
-Vdc/6	0	0	0	0	1	1	1	1	1	1	0	0
-Vdc/3	0	0	0	0	0	1	1	1	1	1	1	0
-Vdc/2	0	0	0	0	0	0	1	1	1	1	1	1

3.0 DESIGN OF INVERTER CONTROL CIRCUIT

The inverter control circuit comprises sine wave generator of 0 and triangular wave generator of amplitude of 0 to1, 1 to 2, 2 to 3, 0 to -1, -1 to -2 and -2 to -3; comparing circuit (Op-Amp) and switching (MOSFET) circuit. The type of inverter implemented in the system is voltage–source–inverter (VSI) and the control technique implemented in the system is sinusoidal pulse width modulation (SPWM) scheme.

Fig. 3 shows the generation of eight PWM for phase 0° using sine wave of 0° phase shift to combine with six triangular waveform of amplitude 0 to1, 1 to 2, 2 to 3, 0 to -1, -1 to -2 and -2 to -3. The results of the combination generate six PWM. When these six PWM are inverted, six additional inverted PWM is generated. The output of these twenty-four PWM is fed into the switches (MOSFET) of the single-phase seven-level DCMLI to generate a modified sine wave AC voltage output. The logic conditions for the switching MOSFET are shown in equations (1) to (12).WhenV_t is the sine wave voltage and V_{m1} to V_{m12} are voltages for the four triangular wave of; 0 to 1, 1 to 2, 2 to 3, 0 to -1, -1 to -2 and -2 to -3respectively. The logic conditions for the eight MOSFET to switch are:

If Vm1 ≥ Vt then A state is ON (1)
If Vm2 >Vt thennotA state is ON (2)
If Vm3 ≥ Vt then B state is ON (3)
If Vm4 >Vt then notB state is ON (4)
If Vm5 ≥ Vt then C state is ON (5)
If Vm6 >Vt then notC state is ON (6)
If Vm7 ≥ Vt then A1 state is ON (7)
If Vm8 >Vt then notA1 state is ON (8)
If Vm9 ≥ Vt then B1 state is ON (9)
If Vm10 >Vt then notB1 state is ON (10)
If Vm11 ≥ Vt then C1 state is ON (11)
If Vm12 >Vt then notC1 state is ON (12)

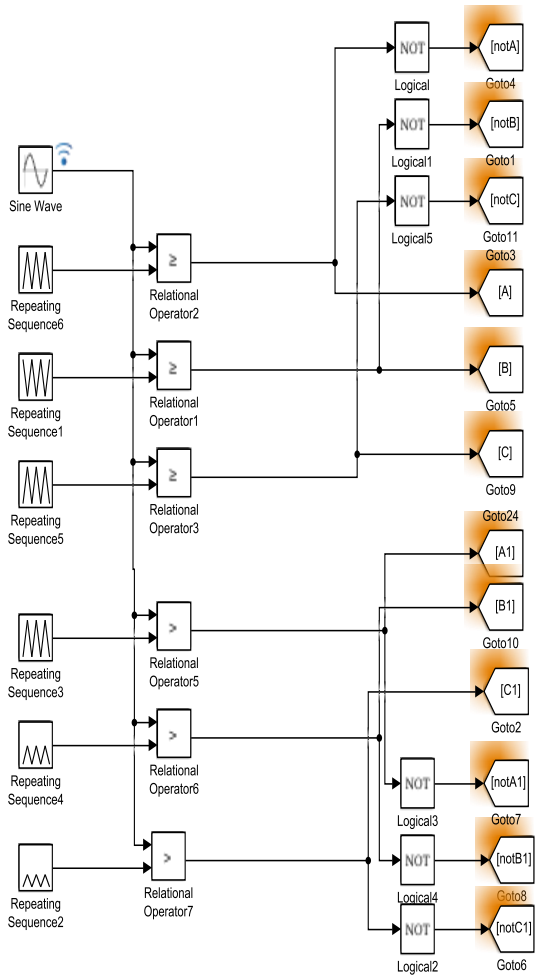

Figure 3: Sinusoidal reference and triangular carrier waves of APOD SPWM for gating pulses

4.0 THD SIMULATION OF THE SINGLE-PHASE SEVEN LEVEL DCMLI FOR PD, POD AND APOD AT M.I = 0.6 TO 1.0 USING MATLAB/SIMULINK

The THD for the DCMLI was simulated for PD, POD and APOD SPWM techniques at varying modulation index of 0.6 to 1.0. The waveforms are as presented in Fig. 4 to Fig. 7.

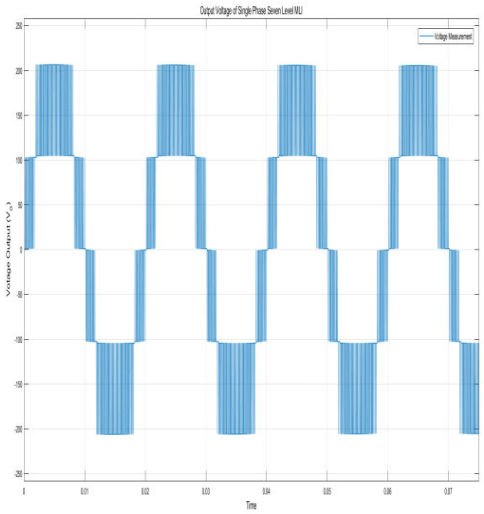

Figure 4: Voltage Output of a Single-Phase Seven-Level DCMLI on no load at m=0.1 to 0.7 for POD PWM

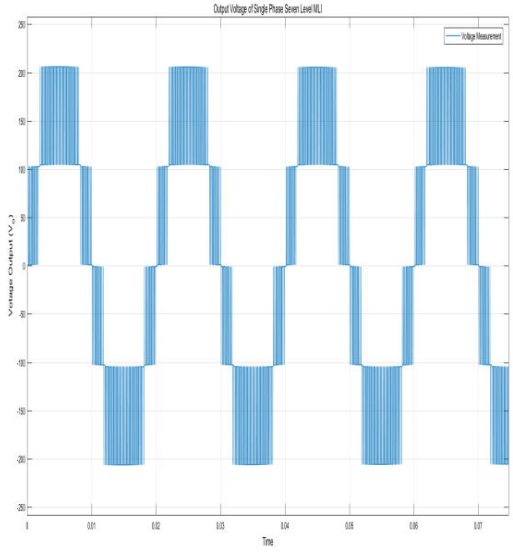

Figure 5: Voltage Output of a Single-Phase Seven-Level DCMLI on no load at m=0.6 for PD PWM

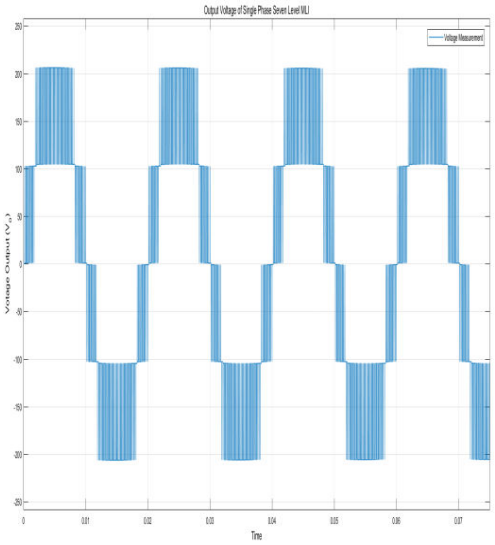

Figure 6: Voltage Output of a Single-Phase Seven-Level DCMLI on no load at m=0.6 for POD PWM

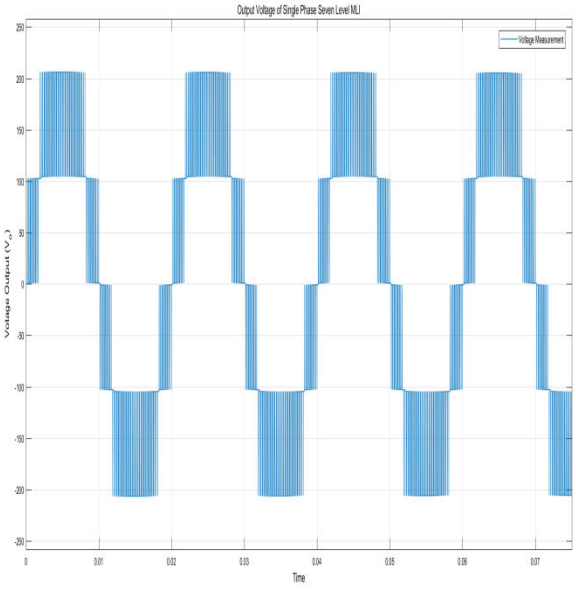

Figure 7: Voltage Output of a Single Phase Seven-Level DCMLI on no load at m=0.6 for APOD PWM

4.1 THD simulation of the single phase seven level DCMLI for PD, POD and APOD at M.I = 0.6 to 1.0 using MATLAB/SIMULINK

The results from frequency analysis of PD, POD and APOD are summarized in Table 2 to Table 4.

Table 2: THD and Fundamental magnitude of PD PWM technique of 7 level DC MLI

Modulation Index (M.I)	Fundamental Mag (50Hz)	Total Harmonic Distortion (THD) %
1	311.2	17.93
0.9	280.2	22.11
0.8	249.1	23.97
0.7	217.4	24.86
0.6	186.1	32.88

Table 3: THD and Fundamental magnitude of POD PWM technique of 7 level DC MLI

Modulation Index (M.I)	Fundamental Mag. (50 Hz)	Total Harmonic Distortion (THD) %
1	311.2	17.92
0.9	280.2	22.09
0.8	249.1	23.96
0.7	217.4	24.84
0.6	186.1	32.86

Table 4: THD and Fundamental magnitude of APOD PWM technique of 7 level DC MLI

Modulation Index (M.I)	Fundamental Mag. (50Hz)	Total Harmonic Distortion (THD) %
1	311.2	17.89
0.9	280.2	22.12
0.8	249.1	23.97
0.7	217.4	24.85
0.6	186.1	32.82

From Table 2 to Table 4, it shows that the modulation index of 1.0 has the lowest THD values of 17.93 %, 17.92 % and 17.89 % respectively with fundamental frequency amplitudes of 311.2 for PD, POD and APOD SPWM in the FFT analysis of the single phase seven level DC MLI. This shows that APOD SPWM techniques has better THD performance than PD and POD in a single phase seven level DCMLI due to low THD percentage recorded as 17.89 % with a magnitude of 311.2 over 3 cycles at a fundamental frequency of 50Hz over a maximum frequency of 1kHz.

5.0 CONCLUSION

In this work, a design and development of a Single-phase Seven-level Diode Clamped MLI using PD, POD and APOD SPWM technique has been achieved. The THD of the output of the inverter was observed to have the lowest THD of 17.89 % at a modulation index of 1.0.on no load.

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